EE 741

Power Flow in Distribution Systems

Power Flow

- Purpose: determine the following:
 - Voltage magnitudes and phase angles at all nodes
 - Current and power flow in each line section
 - Power loss in each line section, and total power loss
 - Total feeder input power (MW, MVAR)
 - Load MW and MVAR based on specified model
- Solution technique
 - Iterative techniques commonly used in transmission network studies (e.g., Newton Raphson, decoupled Newton Raphson, Gauss-Seidel) are not used because of poor convergence characteristics.
 - Instead an iterative technique (i.e., forward/backward substitution) specifically designed for a radial system is used.
 - Refer to Gridlab-D or OpenDSS course slides on power flow module.

Example of forward/backward substitution

• Source voltage at Node 1: 7,200 V

 $S_2 = 1500 + j750$ $S_3 = 900 + j500$ (kW + jkvar)

• Assume voltage at Node 3 = 7,200 V

- Calculate I_{23} , then voltage at Node 2, then current I_{12} , the voltage at Node 1

 $V_1 = V_2 + Z_{12} \cdot I_{12} = 7376.2 / 0.97 \text{ V}$ Error = $||V_s| - |V_1|| = 176.2 \text{ V}$

- Error greater than tolerance (0.001 p.u. or 7.2 V) forward substitution:
- Start with voltage at Node 1 = 7,200 V, use line currents calculated previously to compute the voltages at the other nodes

 $V_2 = 7085.4 / -0.68 \text{ V}$ $V_3 = 7026.0 / -1.02 \text{ V}$

 The iteration will be repeated using the new voltage at Node 3 above till, etc. until the error falls below the tolerance.

Example – IEEE 4-Node Feeder



- The infinite bus voltage is balanced 3-phase of 12.47 kV
- Line segment 1-2 is a 3-wire Delta, 2000 ft. long (see pole configuration below). Line segment 3-4 is 2500 ft. long with same pole configuration but is a 4-wire Wye). The lines consist of 336,400 26/7 ACSR phase conductors and the neutral conductor is 4/0 6/1 ACSR (refer to previous examples for cable data).
- The transformer bank is Delta-Wye grounded that consists of 3 single phase transformers.
 2000 kVA, 12.47 - 2.4 kV, Z = 1.0 + j6.0%
- load data: $S_a = 750$ kVA at 0.85 lagging power factor $S_b = 1000$ kVA at 0.90 lagging power factor $S_c = 1250$ kVA at 0.95 lagging power factor



Example – IEEE 4-Node Feeder

• The iterative process converges after 4 iterations, and the final phase voltages at Node are

$$[V4_{\text{final}}] = \begin{bmatrix} 2278.7 / -31.8 \\ 2199.8 / -153.5 \\ 2211.2 / 83.1 \end{bmatrix} V$$

• Assignment # 4. Use OpenDSS to verify the above