A NEW PARALLEL ARCHITECTURE TO DEAL WITH REAL-TIME COMPUTER IMAGE PROCESSING

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Abstract: This paper will describe an architecture composed by specific cells real-time image processing oriented. The architecture has an optimal relation cost/efficiency, modularity, application based dynamic re-programmability as well as the facility of interconnection, extension, and synchronisation of the system, that makes possible the interchange of information between any pair of cells of the network. This architecture is design to be able to carry out parallel operations in computer vision processes, specially in the phases of pre-processing, processing and recognition.

Keywords: parallel architecture, real-time processing, image processing, quality control inspection

1. INTRODUCTION

Modern control systems are based in RTOS running under PC environments. In general, using such software OS, real-time operation is constrained by acquisition and pre-processing tasks of input signals. An extremely example arrives when dealing with cameras and snapped images as basic sensors. In such a problems, specific pre-processors can be used.

When the capacity of the board is overlapped, the application require a parallel architecture in order to deal with real time image processing.

In computer vision the tasks can be grouped in different levels: Image capture, Signal processing, Image processing, Image post-processing, Image interpretation [1].

The first level is associate to the sensorial part of capture of the image (B/N or colour), and generates the synchronism.

The second level can be defined as a stage of pre-processing of the signal. The modules that integrate it generate new processed images that allow to apply the next processing algorithms.

These are some of main the operations associated at this level:

- **Binary image**: generate a first segmentation of the image.
- **Re-histogram**: it consists of applying non-linear transformations on the different levels of grey of the image.
- **Filtrate**: Application of operators with the purpose, for example, to reduce the effects of the noise.

The third level, known like image processing, consists of operations such as the restoration of contours or images, which are considered, together with the pre-processing functions, like previous stages to extract the characteristics.

Fourth level, the one of post-processing or recognition, is considered as a previous stage of interpretation. In this level the algorithms for detection, location and recognition are implemented.

At the last level we are able to interpret scenes, entering in the field of artificial intelligence, and this implies capacity to compare the sensorial information and of the previous available knowledge. We must incorporate in this level the capacity to learn and to extend the data bases of the knowledge.

The paper presents an open architecture that allows to execute the functions described before, individually or chained [2], as well as other future ones related to the computer vision.

2. ARCHITECTURE'S REQUIREMENTS

We following describe the basic premises that conditioned the design of the architecture. The processes can be executed in individual cells or can be grouped and executed in parallel [3]. Of course, each cell or group of them will have to be
This are the basic requirements of the architecture's:

1. The elementary cells must have an optimal relation cost/efficiency. The system should be easily re-programmable, multipurpose and modular.
2. In situations in which the application requires it, any processor will be able to treat like entrance the image provided by any other processor about the matrix, although some options of interconnection can limit the capacity to execute processes in parallel.
3. All the processors must operate in transparent way, being able to directly transfer the input video signal when it is coming out.
4. The only relation between two processors will be at level of image, transmitted pixel by pixel, sharing the signals of video synchronism.
5. Pipeline is allowed between any number of processors, as well as the execution of parallel processes from different images from entrance. The architecture is in fact an assembly of processors that can work independently.
6. Each processor will manage its own memory banks.
7. One will have a dual-port memory that it will operate in way direction shared by all the processors.
8. The control processor will have to be able to provide external synchronism exits for the control of cameras.
9. It must be contemplated to the possibility of several entrances and exits of video of 3 channels, specially to process images RGB.
10. The architecture must easy to expand and realistic in its implementation.

3. RECONFIGURABLE PARALLEL COMPUTER

We propose a parallel, re-configurable architecture based of a systolic array of processors presented in the figure 1, that fulfils the specifications presented before.

- Pro2 processor is in charge of the communications with host.
- Pro1 computer is in charge of the control of the cell.
- A matrix of cells or basic processors [ Pij ] interconnected by means of a network to crossbar of video cells address that we will denominate [ dvij ].

This network allows any interconnection between processors, which can receive or send images pixel by pixel, through an 8 bits bus, which also will be used to send information to host of precise form, through Pro2.

3.1 Video Inputs/Outputs

The architecture has different inputs/outputs that allow RGB cameras to be used without limit the connection to a one channel camera. Due to this propriety, more than one image taken from different cameras can be parallel processed.

Every block A/D incorporates a converter Philips TDA8709A and an extractor of synchronism LM1881, which will be provided to the Pro1 processor, in order to control the cells of the network.

Conversion D/A is done by integrated circuit TDA8702.

3.2 Video signal transport, crossbar

The video transport units, [ dvij ] (video address), are logic programmable, and they facilitate the transmission of digital video signal between different processors [ Pij ] of the network.

In this architecture we can differentiate between the use of input/output units, that control a bus of digital video of 3 channels (in principle of 8 x 3 bits), and the rest of the network units that control a bus of video of a single channel (8 bits).

Figure 2 shows a simplified scheme that gives idea of the necessary number of I/O pins. The programming and control bus word will be in principle of 10 bits, 4 of them will be used to select anyone of the twelve possible configurations of commutation. If we thought about an architecture that integrates initially 64 basic units of process, the 6 remaining bits will be used to identify the physical position (x,y) of the cell [ dvij ] between the 64 possible ones, and be able to carry out their programming. This number can seem an important restriction of the architecture.
The power of the used device FPGA, allows to carry out functions of control to local level, so that two or more groups of devices [dvij] could collaborate, and, if it is necessary, it can disconnected the general bus of the architecture.

3.3 Pij cells
The architecture allow an un-predefined number of homogenous processors, that are linked with the input/output devices through the video signal control blokes [dvij].

To facilitate the implementation and programming the system we propose a homogenous architecture composed by identical processors and powerful enough to handle imagine processing problems.

The specific cell is based on FPGA and DSP devices, processors used in real time operation.
As can be seen in figure 5, the proposed basic processor cell is composed of the following modules:

- A Ping-Pong memory.
- A processor P1 for computation functions.
- A processor P2 for communications and internal dual-port memory control.

Since P1 will be in charge of mathematical operations, we suggest using a DSP processor like the DSP TMS320C51x. Processor P2 will be in charge of initial loading program functions, intercommunications with other processors and the internal Ping-Pong memory management. The memory addressing needs can be managed using, for instance, a FPGA device Altera FLEX10K100A, which will provide computational support for the DSP as well. A typical operation is performed with P2 being in charge of loading M1 while P1 performs computational tasks on M2 memory.

Although additional information about the board can be obtained from the On-line conference of OSEE [4].

4. APPLICATION

As an example we would like to present how to deal with a real application. A video fault detecting system has been implemented in order to provide a quality control and position control of the metal pieces on the conveyer belt.

The pieces are passing in front of a video camera, the captured image is processed using a two layers parallel architecture, one layer used for quality control and the other one for position control.

The faults to be detected are: broken corner, missing of a hole, straightness of the edges. In order to detect the faults mentioned before, the image is processed taking advantage of real-time characteristics of FPGA and DSP processors. For the image to be easy to process it is first transform in a binary image that will be next filtered. At this point the image is ready to extract all the information that we need for computing the parameters. The parameters to be compute are:

- The bounded box, the distance between the four extreme points of the perimeter of the piece.
- The aria.
- The numbers of holes.
- The straightness of the edges.

The bounded box is used in order to determine if the image contain the whole metallic piece. In case that the image doesn’t contain a region with the bounded box equal with the set one, it is not valid and it will not be taken into consideration.

The aria can be computed as a sum of the number of black pixels appearing in the valid binary image.

The number of holes can be determined counting the numbers of different regions from the image. We can distinguish 8 regions: the background, the piece, and 6 holes. The result of the region growing segmentation [5] algorithm is a number of regions in the image. If a hole is missing this number will be less then the total number of regions.

A fault can appear at the edges of the piece. It can be detected comparing the edge with the straight line that is obtained by unify the two corners of the bounding box.

First cell P11 will capture, threshold, filter the image and compute the aria and bounded box parameters. The resulting image is stored in one of the two memories of the cells P12 and P21.

The algorithms for computing the other two parameters are implemented in the DSP of the
Figure 7. Three cells architecture

P12 cell. The output of this cell will be a signal containing the decision concerning the quality control which will be further more send to the PC.

The position control algorithm is implemented in the third cell P21, and the result is send to the PC.

The outputs of the boards P12, P21 are synchronised and there is the possibility to be directly send to the control architecture of the system.

5. CONCLUSIONS

When dealing with cameras as external sensors, a computer hardly can handle image processing and control at the same time, even using RTOS like as VxWorks or QNX. In applications like online quality control or, for example, autonomous navigation, working at a video rate it is still an open subject. In both cases, the image interpretation and a high level of intelligent control is difficult to be done at video rate.

When talking about quality control in real-time, commercial boards can be used. However, such boards are running usually under Windows environment and is well known that many pre-processing tasks can be executed to a video rate, but this can be difficult when is dealing also with artificial intelligence concepts that need a long computation time. In this cases the proposed architecture from figure 1 allows a level of processing that cannot be found through the present commercial products.

The figure 8 presents a pipeline computer based on two basic cells. The possibility of interconnecting a big number of cells gives to this architecture an unlimited processing power.

When considering the video image as a key-information, the presented idea takes advantage of the specific real-time hardware system, for reducing the number of tasks carried out by the PC, improving in this way the response time. An example can be consider also in the field of mobile robots where the control behaviour architecture is executed using the PS which is in charge of all the tasks, from logging sensor readings until the intelligent control architecture.

6. REFERENCES


